



Evolving DDR Platform

Mobile

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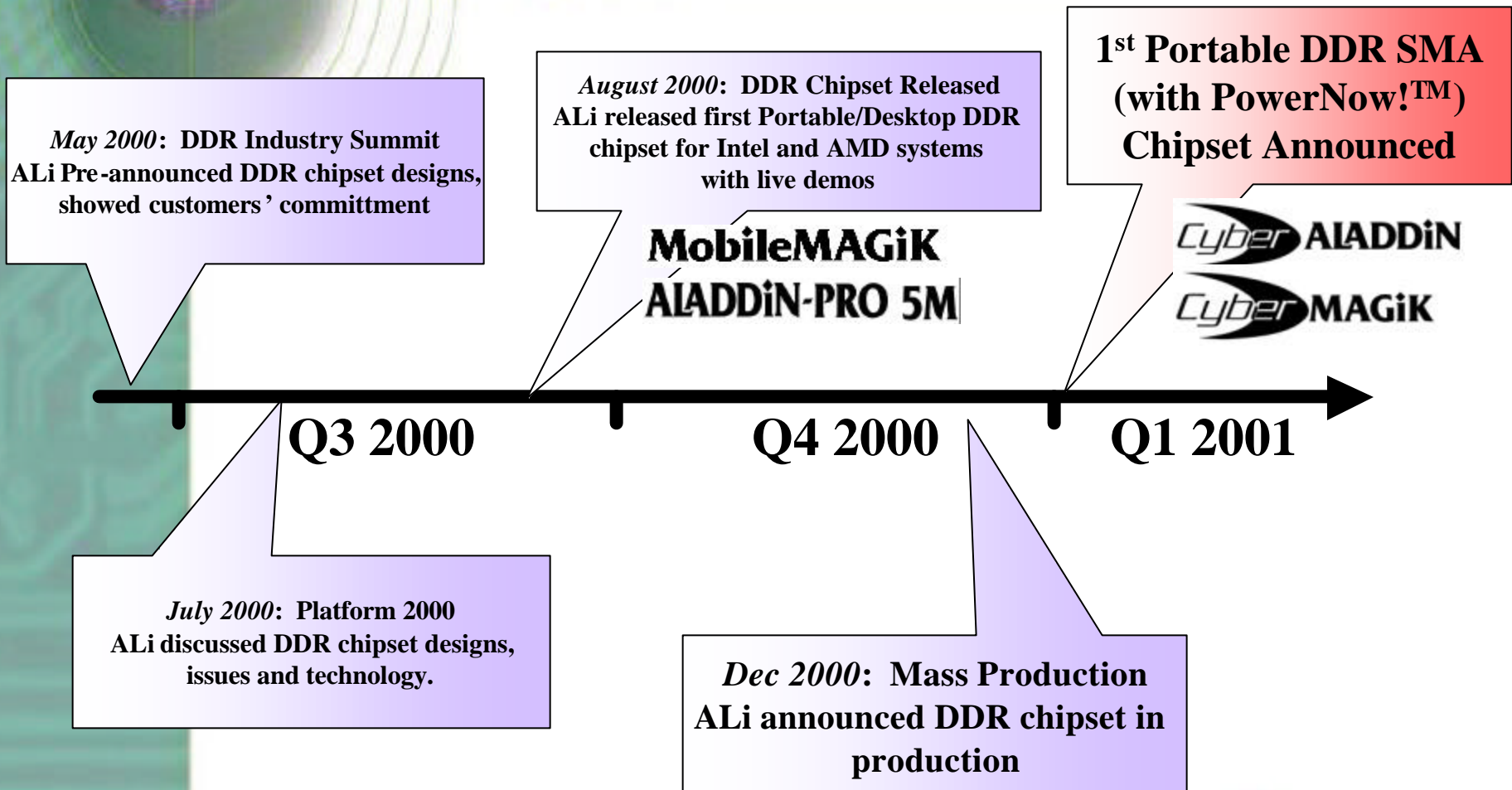
Agenda

- ✍ **ALI DDR Commitment**
- ✍ **ALI DDR Chipset Market Positioning**
 - ✍ **DDR Review**
 - ✍ **ALI's DDR Chipset Offerings**
- ✍ **Introducing First Portable DDR SMA (with PowerNow!™) Chipsets**
 - ✍ **For AMD Socket A CPUs**
 - ✍ **For Intel Socket 370 CPUs**
- ✍ **Conclusion**

Cyber MAGiK

Cyber ALADDiN

ALi's DDR Commitment



Key Features: DDR vs SDR

	DDR	SDR (PC133)
Clock Frequency	up to 133MHz differential clock	up to 133MHz single-ended clock
Bandwidth	2 Gbytes/sec	1 Gbytes/sec
Signal Level	2.5V SSTL-2	3.3V LVTTTL
Synchronization	Source synchronous Read: edge-aligned Write: center-aligned	Global clock
Bus Terminator	Serial + Parallel resistor	N/A
Input PAD	Pseudo differential	Single-ended
CAS Latency	Read: 2/2.5 Write: 1	Read: 2/3 Write: 0
SO-DIMM (portable) Mechanicals	200 pins Same footprint as 144- pin PC-133 SO-DIMM	144 pins

ALi's DDR Chipset Offerings

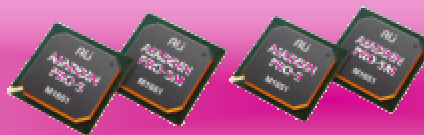
MobileMAGiK ALADDiN-PRO 5M
M1647 M1651

- ✍ **1st SDR/DDR chipset for both AMD and Intel CPUs for mainstream PCs**
 - ✍ **Leading chipsets for AMD Mobile Athlon CPUs and Intel Portable CPUs**
 - ✍ **1st Mobile DDR chipset**
- ✍ **1st Mobile Athlon chipset with PowerNow!™ Technology**
- ✍ **1st to support Athlon with FSB 266**
- ✍ **Commonality of driver across the board for future integration path and continuous graphics core**



ALi's Current Mobile Chipset Position

Performance



Stand alone MobileMAGiK
& ALADDiN Pro5M



CyberMAGiK & CyberALADDiN
with DDR memory

Mainstream



CyberMAGiK & CyberALADDiN
with SDR memory

Value



ALADDiN CyberBlade i1

DDR SO-DIMM Compatibility List

- Micron
- Samsung
- Hitachi (Elpida)
- Hyundai
- More in progress...

Introducing ...

World 1st Portable DDR SMA (w. PowerNow!™) Chipsets

- ✍ 1st mobile DDR chipset with 128 bit 3D graphic integration for both AMD and Intel CPUs.
- ✍ Same proven core logic features with

MobileMAGiK ALADDiN-PRO 5M

- ✍ Cover the value, mainstream and the performance segment

CyberMAGiK

for



CyberALADDiN

for



CPUs



Acer Labs

Marriage of Proven Technologies

CyberBlade XP

 **Trident**

*Cyber*BLADE XP

M1647 - Standalone Corelogic

 **ALi**

MobileMAGiK

ALADDiN-PRO 5M

M1646
Cyber **MAGiK**

Cyber **ALADDiN**
M1644

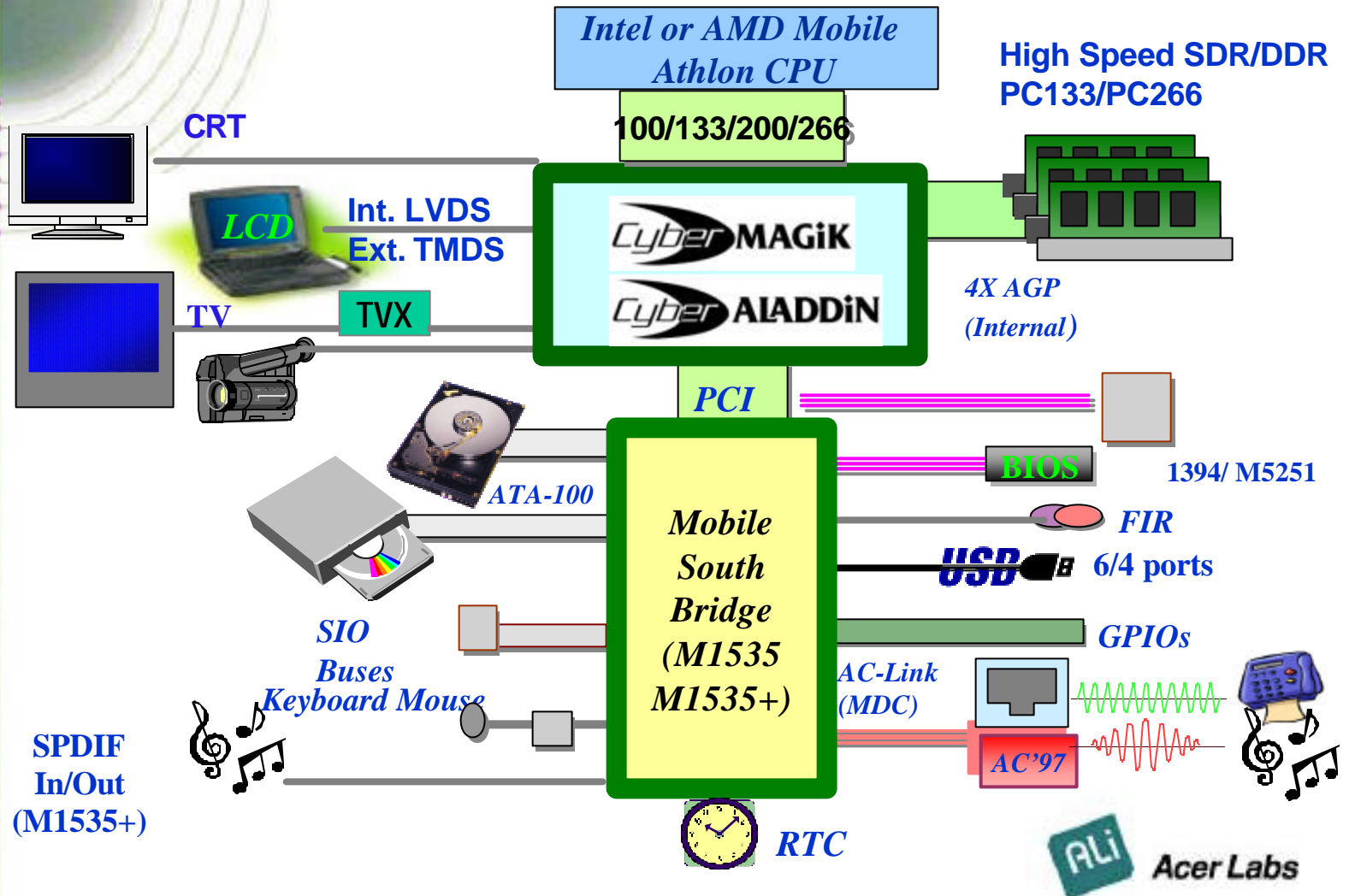
M1651 - Standalone Corelogic

4xAGP, PC133 and DDR

BIOS: 1121a load advance default

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ALi's Mobile DDR SMA Platform





Why choose CyberMAGiK & CyberALADDiN

- Cost Benefits
- Power Benefits
- Performance Benefits
 - Core Logic
 - Graphics



Cost Benefits

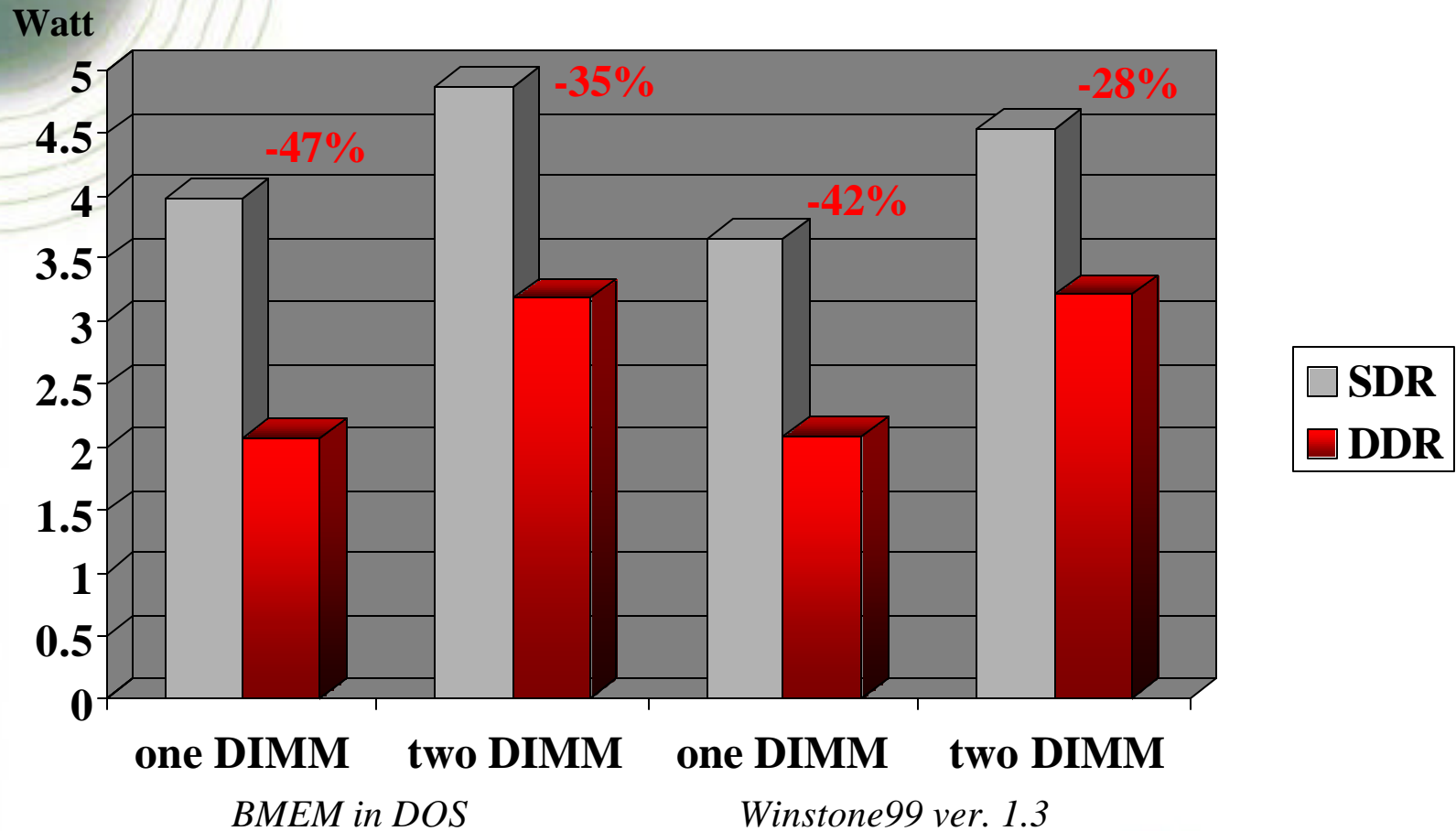
- Low component count to optimize system cost
- SDR Platform for value segment can be leveraged to DDR Platform for mainstream & performance segments to reduce engineering cost



Power Benefits

- DDR operates in lower voltage (2.5V) than SDR (3.3V)
- PowerNow!™, ACPI, SMI, SMM, SMBus for optimum power management

Power Comparison: DDR vs SDR





Best Power Management Southbridge Solution

For Design Flexibility and Extended Battery Life

- ACPI 1.0 and 1.0b Compliant
- SMBus 1.0 and 2.0 compliant
- SMM & SMI Support including SMM Legacy
- Extensive GPIO and Extended GPIO
- PCI Clock run# and Dynamic Stop Clock
- Hot Key and Watch Dog Timer
- Extensive External Wake-up States
- Extensive Timers and System Activity Monitoring
- PowerOn-Suspend, Suspend-to-Disk, Suspend-to-DRAM
- Support 8-Mbit ROM size

Driving for High Performance

Key Features Highlights:

- 266 MHz Double Data Rate (DDR) memory support (2.1 GBytes/sec), PC2100
- SMA 128-bit Architecture with DDR to improve bandwidth
- 200/266 MHz (AMD) FSB & 133 MHz (Intel) FSB support
- DX7.0 Compatible Graphics Accelerator (CyberBlade XP 128-bit Core)
- Proven Building Blocks from ALi and Trident
- Integrated LVDS for LCD panel up to UXGA
- Complies with PC99 and PC2001 spec.

Summary: Highest Level of Integration for Mobile Platform

CyberMAGiK, CyberALADDiN

- 128 bit Dual-Pipe 3D / 2D Graphics
- DVD /MPEG 2 with Motion Comp and iDCT
- LVDS Integration
- Intel™ Mobile Processor Supported
- Supports 4,16,64,128, 256, 512-Mbit SDRAM and/or DDR
- Supports 6 memory rows per byte access on each row
- Supports LVTTL/SSTL signal level
- Dynamic switching CKE algorithm for low power
- Shared Memory Interface: 4MB, 8MB, 16MB, 32MB (**no frame buffer required**)
- PowerNow!™, ACPI, SMI, SMM support
- 555 Pin BGA (35mmx35mm)

M1535+ Mobile Southbridge

- Support Ultra DMA Mode Transfers upto Mode 5 timing (100 Mbytes/sec - ATA 100)
- Consumer SPDIF Input/Output
- Six (6) USB ports with two (2) USB controllers based on OpenHCI 1.0a specification
- ACPI 1.0/1.0b, SMBus support
- AC-Link Host controller compliant with AC'97 2.1
- HSP Modem Solution
- Hardware SoundBlaster Pro/16 compatible legacy audio
- 352-pin (27mmx27mm) BGA package

Trident Microsystems

- 14 yrs in Graphics business since **1987**
- 1997: First **DVD** solution for Desktop PC
- 1999: First **Graphics + Core Logic** for Notebook
- 2000: First **DX 7.0** solution for Notebook
- 2001: First **Graphics + Core Logic** with **DDR**
- Claim-to-fame: **Performance Per Watt**

Major OEM / ODM Notebooks

Acer  **COMPAQ**

Arima

FUJITSU

IBM

 **COMPAL**


invent

HITACHI

NEC

 **MITAC**

SONY

TOSHIBA

Quanta Computer

Powered By Trident 3D Graphics

 **Acer Labs**

Notebook Trends

- Expansion of Integrated Graphics/Core Logic Solutions into Mainstream Systems
- TFT LCD's with Enhanced Resolutions and Sizes
- System Memory Migrating to DDR
 - Price parity with SDR
- Desktop Gaming Experience on Notebook



Notebook Roadmap

Notebook Segment

Professional
>\$3.0K

Mainstream
Performance 3

Mainstream
Performance 2

Mainstream
Performance 1

Value
<\$1.5K

Notebook Production Cycle

Q2'00

Q3'00

Q4'00

Q1'01

Q2'01

- * 128-bit Dual-Pipe 3D
- * AGP 4x
- * DVD MC & iDCT
- * Dual LCD
- * CS NOW, MP 11/00

CB XP

Blade XP Core

Discrete

CB XP
m8
m16

MCM

- * 8MB or 16MB
- * CS NOW

Blade3D Core

*Integrated
Core Logic*

Trident/Via
CB i7
(AMD)

- * VIA Socket 7
- * NB + SMA
- * MP NOW

Trident/ALi
CB Ai1
(Intel)

- * CyberBlade3D + ALi NB
- * Shared Mem (SMA)
- * LVDS
- * MP NOW

Trident/ALi
CyberMAGiK
CyberAIADDiN

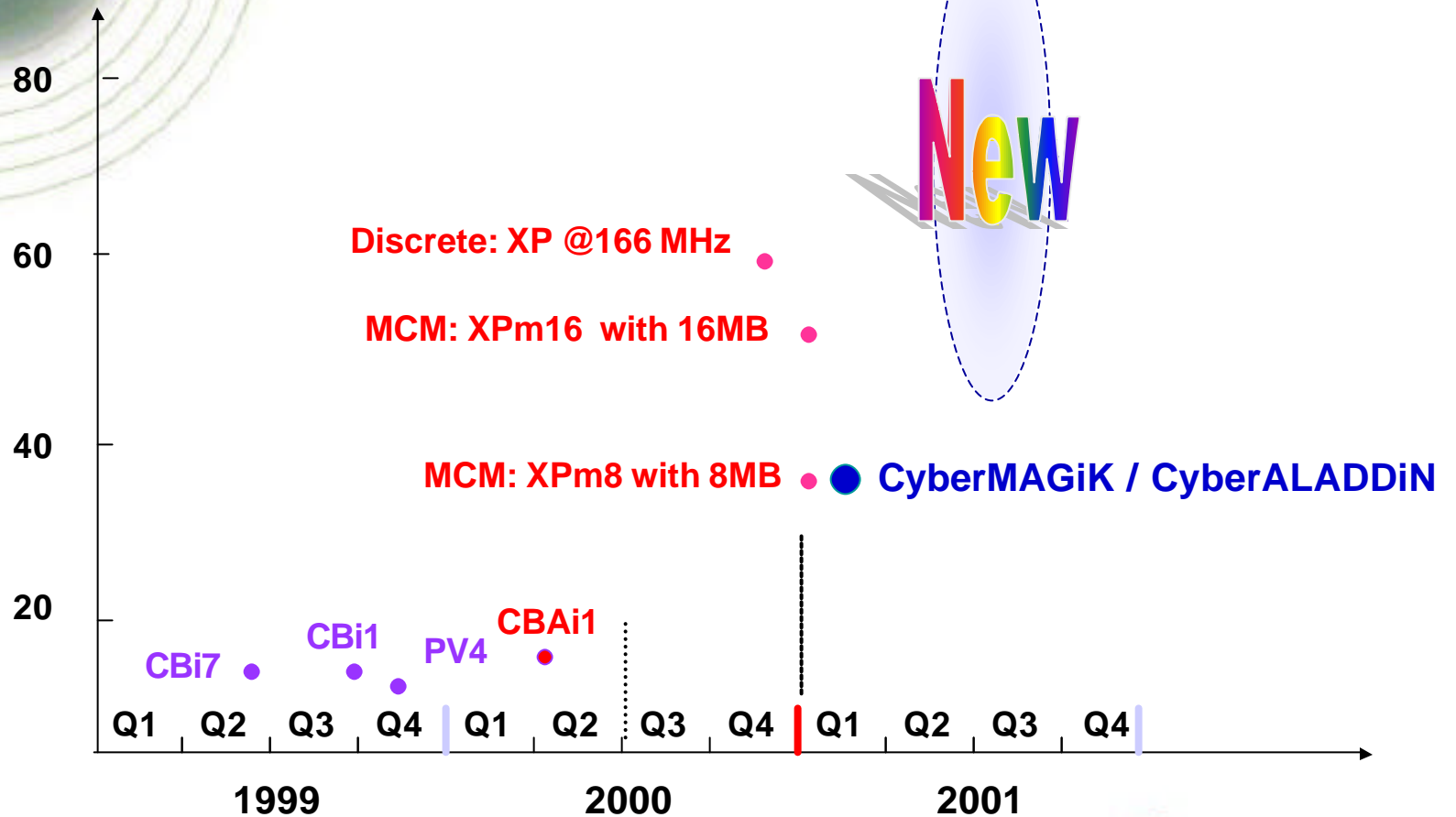
- * XP + Northbridge
- * Shared Memory (SMA)
- * DDR / SDR, LVDS, etc.
- * ES Feb '01, MP 2Q, '01



Acer Labs

Performance Roadmap

3DWB2000 @ 10x7x16-bit



Blade XP Core

- Graphics **Core** for CyberMAGiK and CyberALADDiN
- **DirectX 7.0** with **Cubic** Mapping hardware
- Power dissipation: **1.6 w** (max), **0.5 w** (static)
- Integrated **LVDS** driver with **DSTN** support
- Up to **1600x1200** UXGA resolution for LCD panel
- **Dual** Panel interface
- **State-of-the-art** Video De-Interlacing
- Frame buffer from **4 to 32 MB**
- **128-bit** internal memory interface
- Performance: **2.5X** of competition

3D Overview

	<u>Blade XP</u>	<u>Blade3D</u>
API Support in HW		
DirectX 7.0	Yes	-
OpenGL 1.2	Yes	-
Engine Hardware		
Transformation	SW	-
Lighting	SW + HW	-
Setup Engine	32-bit FP	FP / Integer
Primitive Engine	32-bit FP	Integer
Pixel Rendering Pipelines	Dual 128-bit	Single 64-bit
Accelerated Lighting		
Phong Lighting (per pixel)	Yes	-
Reflections & refractions	Yes	-
Multiple Lights	Yes	-
Guard Band Clipping	X and Y	X only

3D Rendering

	<u>Blade XP</u>	<u>Blade3D</u>
Lighting Model	Diffuse / Specular	Diffuse / Specular
Shading Model		
Enhanced Gouraud	Yes	Yes
Phong-quality	Yes	--
Color Format	16 / 24 / 32-bit	16/24/32
Z-Buffering	16 / 24 / 32-bit	16-bit
W-Buffering	16 / 24 / 32-bit	--
Scene Anti-Aliasing Support	Yes	--
Dithering	Yes	Yes
Stencil Buffer	8-bit	--

3D Texturing

	<u>Blade XP</u>	<u>Blade3D</u>
DirectX 7.0	Yes	--
Single-Pass Cubic Mapping	Yes	--
Single-Pass Bump Mapping	Yes	--
Texture Compression	Yes	Yes
Anisotropic + Trilinear Texture Filtering	Yes	Yes
Texture Size	2K x 2K	1K x 1K
Detail Texture	Yes	--
DirectX 7.0 Multi-Texture Modulate Operations	Yes	--
Multi-Texture Linear Blend Operations	Yes	--
Multi-Texture Add & Combine Operations	Yes	--

3D Texturing (continued)

	<u>Blade XP</u>	<u>Blade3D</u>
Texture Cache	4 KB	4 KB
Texture Format		
Palletized	1, 2, 4, 8 bpp	1, 2, 4, 8 bpp
Non-Palletized	16, 32 bpp	16, 32 bpp
Palette Data Format (ARGB)	565, 1555, 4444	565, 1555, 4444
Texture Tiling		
For Textures with 1 or 2 bpp	16 x 16 or 16 x 8	8 x 8
For Textures with 4 or 8 bpp	8 x 8 or 8 x 4	4 x 4
For Textures with 16 or 32 bpp	4 x 4 or 4 x 2	2 x 2
Texturing Features		
Perspective Correct	Yes	Yes
Per Pixel MIP-Mapping (based on LOD)	Yes	Yes
Transparency (Texture Color Keying)	Yes	Yes
Texture Lit, Modulate, Combine	Yes	Yes

Video

	<u>Blade XP</u>	<u>Blade3D</u>
Color Space Conversion (YUV to RGB)	Yes	Yes
Image Scaling		
Horizontal Interpolation	Up / Down	Up / Down
Vertical Interpolation	Up / Down	Up / Down
Diagonal Interpolation	Up / Down	Up / Down
Edge Recovery	Yes	Yes
Full screen Overlay	Yes	Yes
Video Capture to Frame Buffer	Yes	Yes
Multiple Display Support	Yes	Yes
Chroma and Color Keys on Both Windows	Yes	Yes
Digital Interface to TV Encoder	Yes	Yes

DVD

THAMA tm Technology:

Motion Compensation

Yes

Yes

IDCT

Yes

-

HD0 (1280 x 720 resolution)

Yes

-

DVD Player

Mediamatics

Yes

Yes

InterVideo

Yes

Yes

De-Interlacing

Advanced

Bob & Weave

LCD Panel

	<u>Blade XP</u>	<u>Blade3D</u>
<i>Dual Panel Interface</i>	Yes	-
First Panel Interface		
TFT Interface	18/24-bit	36-bit
Integrated LVDS Drivers	Yes	-
DSTN support	Yes	-
TMDS Digital Interface		
Bus width	12-bit	-
DVI support	Yes	-
Frame rate control	Yes	Yes
Gamma correction	Yes	-
Auto expansion and centering	Yes	-
UXGA resolution (1600 x 1200)	Yes	-
Spread Spectrum Clocking	Yes	-

Performance

	<u>Blade XP</u>	<u>Blade3D</u>
Memory Clock (MHz)	133 DDR	133 SDR
Memory Bandwidth (GB/sec)	2.2	1.1
Graphics Engine Clock (MHz)	133	133
Pixel Per Clock	2	1
Pixel Rendering Rate (pixels/sec)	266 M	133 M
Texel Access Rate (texels/sec)	1,064 M	532 M
DVD Playback Headroom @ 800 MHz P3	60%	50%

Intel™ Mobile Chipset Solution

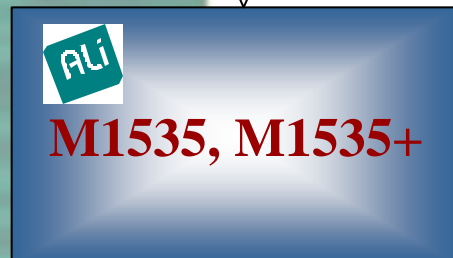


Northbridge:

M1644

For all Celeron, Pentium II and Pentium III processors

- PC-133 SDR/PC-266 DDR
- Clocks: FSB 66/100/133MHz; Memory 66/100/133MHz
- 4 PCI masters with priority setting
- ACPI, SMI support for optimum power management
- Integrated DX7 compatible graphic core (Trident CyberBlade XP)
 - 128-bit internal datapath, Dual pixel pipes, <= 32-bit depth rendering, Motion Comp.
 - HW-Setup, Lighting, Rendering, and Texturing Engines
 - Integrated single-channel LVDS transmitter,
 - interface to external 12/24-bit TMDS
 - Supports up to 1600X1200 TFT panel and 16/24-bit interface to DSTNs



1535, 1535+ Southbridge:

1535 (Available Now)

1535+(Available Now)

- Integrated SIO
- Ultra 33/66/100
- HW Audio (SB)
- AC-97 Support
- SPDIF
- SW Modem



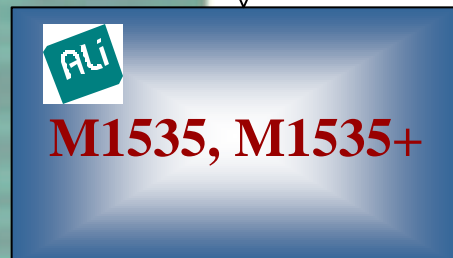
AMD™ Mobile Chipset Solution



Northbridge:

M1646

- AMD K7 Socket-A support
- PC-133 SDR/PC-266 DDR
- Clocks: FSB 200/266MHz; Memory 66/100/133MHz
- 4 PCI masters with priority setting
- PowerNow!™, ACPI, SMI support for optimum power management
- Integrated DX7 compatible graphic core (Trident CyberBlade XP)
 - 128-bit internal datapath, Dual pixel pipes, <= 32-bit depth rendering, Motion Comp.
 - HW-Setup, Lighting, Rendering, and Texturing Engines
 - Integrated single-channel LVDS transmitter,
 - interface to external 12/24-bit TMDS
 - Supports up to 1600X1200 XGA TFT panel and 16/24-bit interface to DSTNs



1535, 1535+ Southbridge:

1535 (Available Now)

1535+(Available Now)

- Integrated SIO
- Ultra 33/66/100
- HW Audio (SB)
- AC-97 Support
- SPDIF
- SW Modem

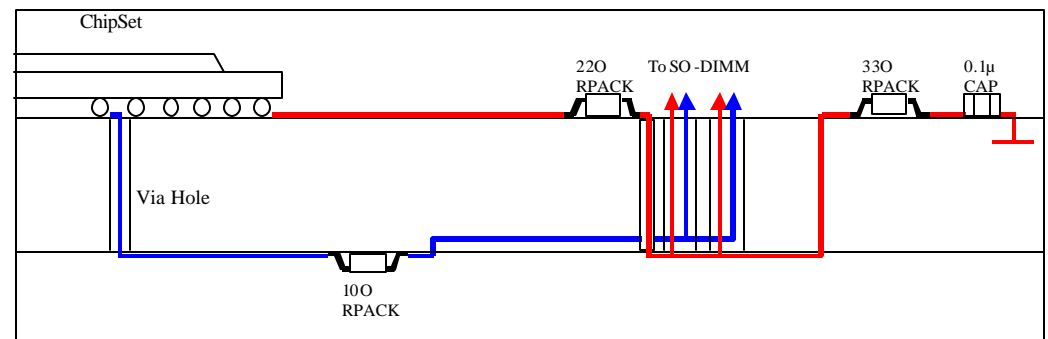
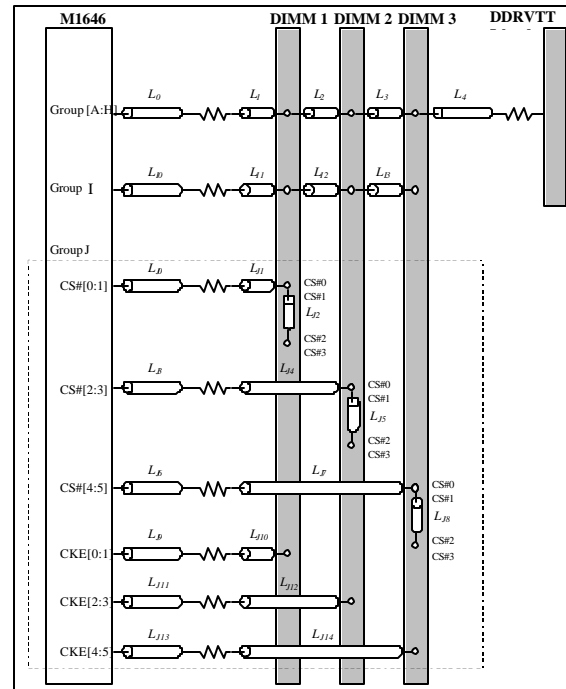
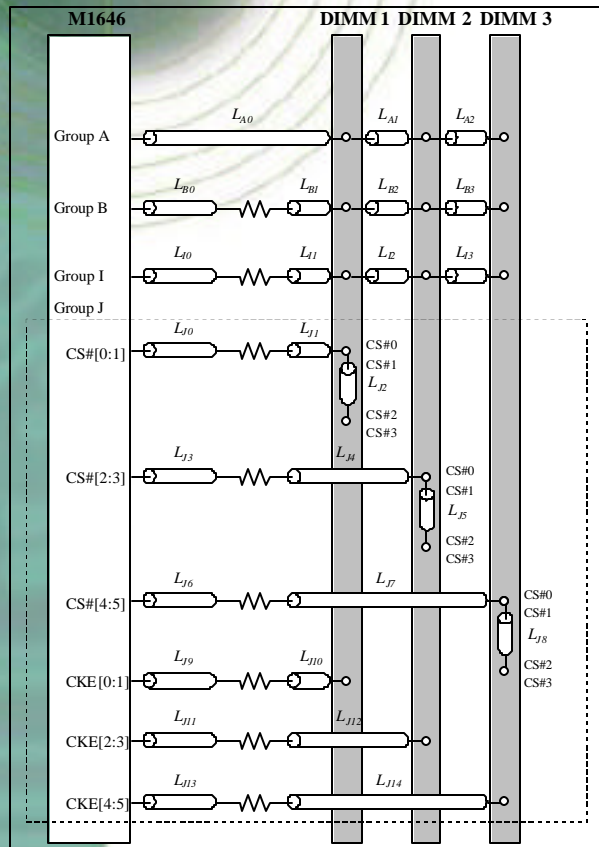




General MB Layout Guidelines

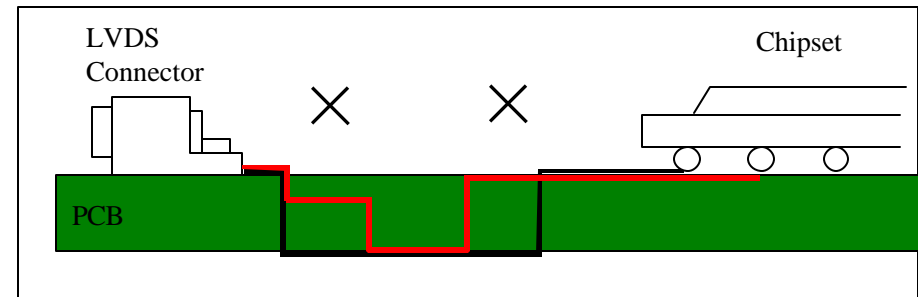
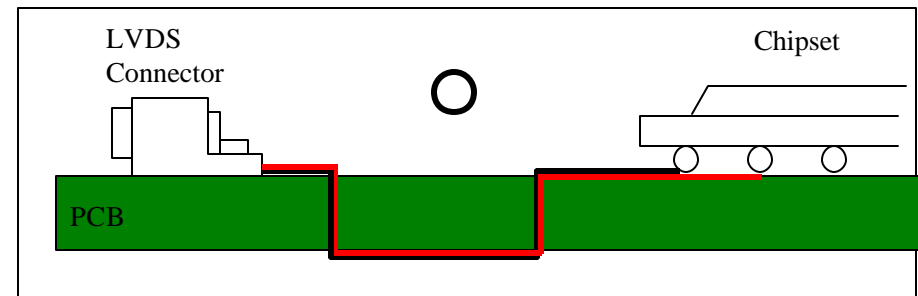
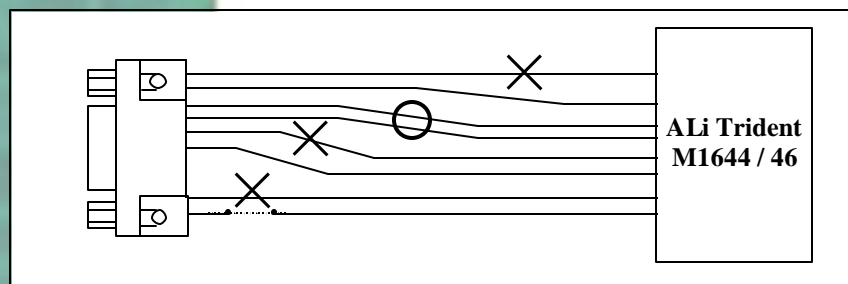
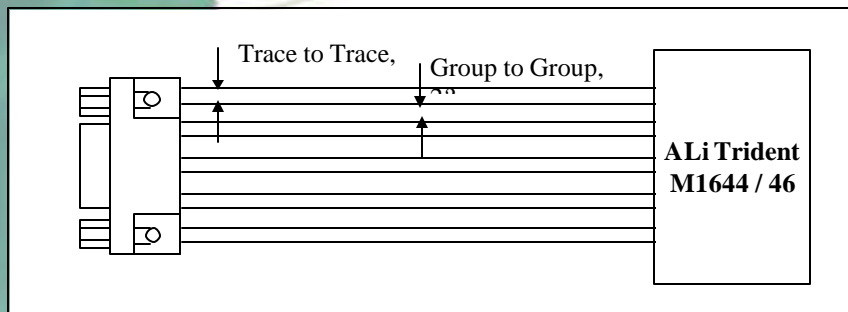
- Do not connect thermal GND pad to big piece of copper on top layer, nor use via holes for V_{CC} and GND
- Maximum trace length difference in each signal-group ≤ 100 mils
- Trace length difference between signal-groups should be < 3000 mils
- Trace length of all signals in clock-forwarded signal-group should be within 1000 to 5000 mils
- Watch for “trace width & spacing” between signal-groups
 - Trace width, spacing to others, clearance to itself

SDR, DDR, SO-DIMM Layout



DFP Layout on MB

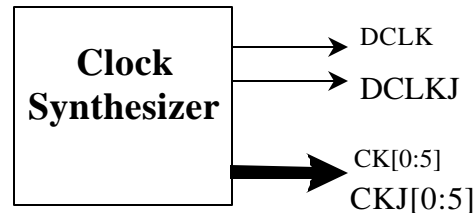
- Length difference of each differential pair should be less than 100mil



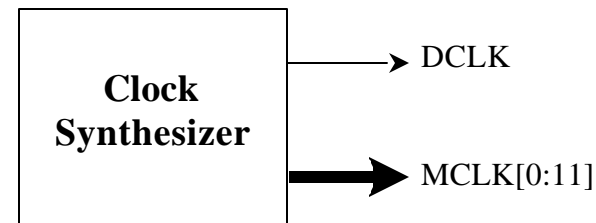
Clocking for DIMMs

- Clock Driver for upto 2xDDR modules directly
- Clock Driver + Buffer for 3xDDR module
 - Feedback path length in total trace-length consideration

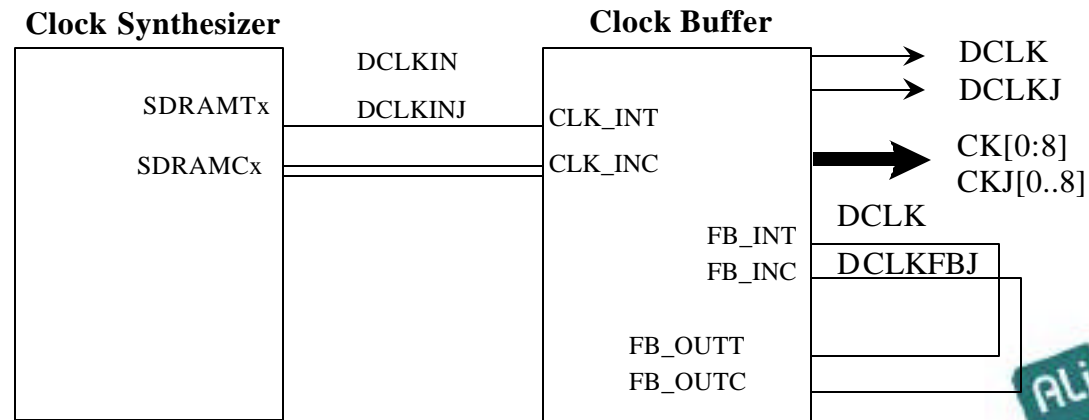
2 DDR SO-DIMM



3 SDR SO-DIMM



3 DDR SO-DIMM



Acer Labs

Conclusion



The choices for mobile DDR platform

- Fully realize the advantages of SMA architecture with DDR technology
- Balances price, power and performance



Thank You!

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